tronic device may then save the values which produced in the highest result signal **324** in their respective registers and proceed with ordinary operation.

[0092] The above discussed initialization process can be performed by channel scan logic **110**. Alternatively, it can be performed by the multi-touch processor which may control the channel scan logic.

[0093] Thus, in general, an embodiment of the invention can include a first signal, which is in general a signal that is to be processed (also referred to as the incoming signal). The embodiment may also feature a demodulation signal which is to be used in conjunction with the first signal in the processing of the first signal. The embodiment may feature one or more processing modules (e.g., analog channels) which process different versions of the first signal.

[0094] The first signal can be the result of an initially generated stimulation signal which passes through various different circuit and/or external sensors (generally referred to as the traversal circuits) to result in the first signal. Thus, the first signal may differ from the stimulation signal depending on the circuits the stimulation signal goes through to result in the first signal. Versions of the first signal arriving at the different processing modules may differ among each other as well as they may pass through different circuits before they arrive at the processing modules.

[0095] In addition, the circuits through which the stimulation signal passes to result in the first signal can change over time. Thus, the difference or the relationship between the initial stimulation signal and the resulting first signal can change with time for any particular processing module.

[0096] This embodiment of the invention provides for demodulation circuitry which generates a demodulation signal in such a way as to ensure that the demodulation signal possesses a specific attribute selected in relation to the first signal. More specifically, the demodulation signal should be generated in such a way as to ensure that it has the same phase as the first signal. This is performed by having each processing module generate its own demodulation signal. At each processing module, the phase of the demodulation signal is controlled by referring to (i) a processing module specific value which refers to the difference in phase contributed to the particular circuit associated with the present processing module, and (ii) a timing specific value, which refers to the difference in phase contributed to temporary factors. The timing specific value may change over-time as the circuits through which the first signal must pass may also change. An example of the timing specific value can be the row specific phase delay value, as in one embodiment the temporary difference of the first signal is caused by the periodic stimulation of different rows.

[0097] The processing module and timing specific values are stored in memory or registers and are accessed as needed to control the phase of the demodulation signal by each processing module. These values can be obtained during an initialization phase by testing various possible values and determining which ones result in the smallest differences in phase between the demodulation signal and the first signal.

[0098] Once the demodulation signal is generated, it is used to process the first signal. The processing can include demodulating, rectifying or performing noise suppression on the first signal. The processing can include combining the first signal and the demodulation signal in a mixer.

[0099] As discussed above, the demodulation signal can be used, to demodulate, rectify and/or perform noise suppression for the incoming signal. Therefore, in general, the demodulation signal is a signal that is configured to perform any one of these functions individually or more than one of these functions together, and is not strictly limited to demodulation.

[0100] In general, when the present disclosure discusses a matching of the phases of two signals, or generating a signal that has the same phase as another signal, it does not require that the phases be exactly the same. A person of skill in the art would recognize that all engineering endeavors include some uncertainty. Therefore, in this case, it should be understood that the phase is only matched within a reasonable degree of error. For example, in an embodiment where the phase of the generated signal is only able to take on discrete values (as is the case when the phase is controlled using a multi-tapped shifter as discussed above), the phase of the generated signal can only match the phase of the incoming signal within an error range related to the gap between the discrete values.

[0101] FIG. **9** is a flow chart showing a method of generating predefined row specific and column specific phase delay values. The method of FIG. **5** can be performed at an initialization stage at time of device manufacture, or during re-initialization operations during the life of the device.

[0102] At step **900**, the process begins. At step **902**, a row count value is set to zero. At step **904**, a current row signified by the row count value is stimulated with a stimulating signal. While the stimulating signal is being applied, the phase of the demodulation signal at each channel is swept so that the demodulation signal periodically changes through all phases producible by the shift register. For each channel, the value of the result signals (see signal **324** of FIG. **3***a*) produced by that channel for each different phase are noted, and the phase which produces the maximum result signal is noted. This maximum result phase can be considered to be the desired phase for the specific row and column combination. At step **906**, the row count is incremented. At step **908**, it is determined whether the row count has reached its maximum value. If the row count has not reached its maximum value the process returns to step **904**, if it has, the process proceeds to step **910**. The maximum value of the row count may be the number of rows present.

[0103] At step **910**, the necessary predefined phase delay values are generated based on the values obtained in the repetitions of step **904**. When step **910** is reached, the repetitions of step **904** have resulted in a desired phase delay value for each row and column combination (i.e., each pixel). These values can be used to populate the various tables which define the different desired phase delay values. For example, all desired values can be copied in a single table (placed in RAM, or in register space) which specifies a desired phase delay value for each row and column combination. In the other hand, in the embodiment discussed by FIGS. **7** and **8**, mathematical operations must be performed on the values obtained in step **904** in order to determine a channel specific phase delay value associated with each channel and a row specific phase delay value associate with each row. A person of skill in the art would recognize how to obtain these values.

[0104] Although the present invention has been fully described in connection with embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications will become apparent to those skilled in the art. Such changes and modifications are to be understood as being included within the scope of the present invention as defined by the appended claims.